IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Canceled).

Claim 2 (Currently Amended): The microprocessor of claim [[1]] 13, further comprising:

an instruction cache memory configured to store a cache line containing a part of the instructions of the program in correspondence to the specific program identifier, and permit reading of the cache line only when the specific program identifier stored in correspondence to the cache line coincides with a program identifier received along with a program reading request from the processor core;

wherein the key management unit is also configured to carry out a flashing of the cache line stored in correspondence to the specific program identifier on the cache memory when the key management unit rewrites the instruction key corresponding to the specific program identifier in the key table.

Claim 3 (Original): The microprocessor of claim 2, wherein the key management unit carries out the flashing in parallel to the key registration, and notifies the completion of the key registration to the processor core when the key registration and the flashing are both completed.

Claim 4 (Currently Amended): The microprocessor of claim [[1]] 13, further comprising:

an instruction decryption processing unit configured to decrypt the encrypted instructions of the program read out from the external memory, by using the instruction key

registered in correspondence to the specific program identifier by the key management unit, according to a chain information indicating chain relationships among encryption blocks in units of which the encrypted instructions are encrypted.

Claim 5 (Currently Amended): The microprocessor of claim [[1]] 13, wherein the key management unit is also configured to register a data key to be used in encrypting/decrypting data for the program in correspondence to the specific program identifier into the key table.

Claim 6 (Original): The microprocessor of claim 5, wherein the key table stores a plurality of instruction keys or data keys which are indexed by key value indexes, and the microprocessor further comprises:

a key index conversion unit configured to convert a set of a program identifier and a key type identifier received from the processor core into a corresponding key value index; and

a decryption processing unit configured to decrypt encrypted instructions or data of a program specified by the program identifier received from the processor core and read out from the external memory, by using an instruction key or a data key indexed by the corresponding key value index obtained by the key index conversion unit.

Claim 7 (Previously Presented): The microprocessor of claim 6, wherein the key index conversion unit converts more than one set of a program identifier and a key type identifier into an identical key value index.

Claim 8 (Original): The microprocessor of claim 6, further comprising:

a cache memory configured to store a part of instructions or data of programs by using key value indexes obtained by the key index conversion unit as cache tags.

Claim 9 (Currently Amended): The microprocessor of claim [[1]] 13, wherein the key management unit is also configured to register a context key to be used in encrypting/decrypting context for the program in correspondence to the specific program identifier into the key table.

Claim 10 (Canceled).

Claim 11 (Currently Amended): ~~The~~ A microprocessor ~~of claim 10,~~ internally having a secret key specific to the microprocessor that cannot be read out to an external device, the microprocessor comprising:

a processor core configured to execute instructions of a program including plaintext instructions and encrypted instructions and to particularly execute a key registration instruction in which a registration request is issued, the encrypted instructions being encrypted by using an instruction key specific to the program; and

a key management unit configured to, when receiving the registration request, carry out a key registration in which a distribution key that is obtained in advance by encrypting the instruction key and a feedback key integrally by using a public key corresponding to the secret key is read out from an external memory, the distribution key is decrypted by using the secret key to obtain the instruction key and the feedback key, and the instruction key and the feedback key are registered in correspondence to a specific program identifier for identifying the program into a key table,

wherein the ~~key management unit registers the meta-level information which is a~~ feedback key ~~to be~~ is used in obtaining a feedback information by encrypting the instruction key when the feedback information is to be written into the external memory at a time of a context saving.

Claim 12 (Currently Amended): ~~The~~ A microprocessor ~~of claim 10,~~ internally having a secret key specific to the microprocessor that cannot be read out to an external device, the microprocessor comprising:

a processor core configured to execute instructions of a program including plaintext instructions and encrypted instructions and to particularly execute a key registration instruction in which a registration request is issued, the encrypted instructions being encrypted by using an instruction key specific to the program; and

a key management unit configured to, when receiving the registration request, carry out a key registration in which a distribution key that is obtained in advance by encrypting the instruction key and a perpetuation flag integrally by using a public key corresponding to the secret key is read out from an external memory, the distribution key is decrypted by using the secret key to obtain the instruction key and the perpetuation flag, and the instruction key and the perpetuation flag are registered in correspondence to a specific program identifier for identifying the program into a key table,

wherein the ~~key management unit registers the meta-level information which is a~~ perpetuation flag ~~indicating~~ indicates whether or not to permit a context saving in which the instruction key is encrypted by using a prescribed secret key of the microprocessor and written into the external memory.

Claim 13 (New): A new microprocessor internally having a secret key specific to the microprocessor that cannot be read out to an external device, the microprocessor comprising:

a processor core configured to execute instructions of a program including plaintext instructions and encrypted instructions and to particularly execute a key registration instruction in which a registration request is issued, the encrypted instructions being encrypted by using an instruction key specific to the program; and

a key management unit configured to, when receiving the registration request, carry out a key registration in which a distribution key that is obtained in advance by encrypting the instruction key by using a public key corresponding to the secret key is read out from an external memory, the distribution key is decrypted by using the secret key to obtain the instruction key, and the instruction key is registered in correspondence to a specific program identifier for identifying the program into a key table, and notify a completion of the key registration to the processor core asynchronously by interruption when the key registration is completed,

wherein the processor core continues executing the instructions during the key registration by the key management unit and starts to execute the program by using the corresponding instruction key after receiving notification of the completion of the key registration from the key management unit.